a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface;

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising resinous material provided over said thin film transistor, said interlayer insulating layer having a leveling surface,

D' Cont'd.

wherein said thin film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer comprises amorphous silicon.

---

5. (Twice Amended) A semiconductor device comprising:

Sub B3

a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first resinous substrate, and a liquid crystal layer therebetween;

D2

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer;

an interlayer insulating layer comprising a resinous material provided over said thin-film transistor; and

at least one pixel electrode provided on said interlayer insulating layer,

wherein said thin-film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, and

wherein said semiconductor layer comprises silicon and is obtained by crystallizing amorphous silicon.

11. (Twice Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first resinous substrate, and a liquid crystal layer therebetween;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface; and

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising resinous material provided over said thin film transistor, said interlayer insulating layer having a leveling surface,

wherein said thin film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer comprises microcrystalline silicon.

12. (Twice Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first resinous substrate, and a ferroelectric liquid crystal layer therebetween;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface; and

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising resinous material provided over said thin film transistor, said interlayer insulating layer having a leveling surface,

wherein said thin film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer comprises silicon and is obtained by crystallizing amorphous silicon.

18. (Twice Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first resinous substrate, and a ferroelectric liquid crystal layer therebetween;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface; and

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising resinous material provided over said thin film transistor, said interlayer insulating layer having a leveling surface,

wherein said thin film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said channel formation region comprises amorphous silicon.

23. (Twice Amended) A semiconductor device comprising:

a resinous substrate having an uneven surface, a substrate opposed to said resinous substrate, and a ferroelectric liquid crystal layer therebetween;

a resinous layer provided on said uneven surface of said resinous substrate and having a planarized surface; and

a thin film transistor provided on said planarized surface of said resinous layer;

an interlayer insulating layer comprising a resinous material provided over said thin-film transistor;

at least one pixel electrode provided on said interlayer insulating layer,

wherein said thin film transistor comprising:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer comprises amorphous silicon.

28. (Twice Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first substrate, and a ferroelectric liquid crystal layer therebetween;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer;

an interlayer insulating layer comprising resinous material provided over said thin film transistor, said interlayer insulating layer having a leveling surface,

wherein said thin-film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, and

wherein said channel formation region comprises microcrystalline silicon.

33. (Twice Amended) A semiconductor device comprising:

a resinous substrate having an uneven surface, a substrate opposed to said resinous substrate, and a ferroelectric liquid crystal layer therebetween;

a resinous layer provided on said uneven surface of said resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer;

an interlayer insulating layer comprising a resinous material provided over said thin-film transistor; and

at least one pixel electrode provided on said interlayer insulating layer,

wherein said thin-film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, and

wherein said semiconductor layer comprises microcrystalline silicon.

D1 Cont'd.